CLAIMS

What is claimed is:

1. A semiconductor integrated circuit for processing a received broadcast signal of a type having a known digital code to acquire the signal, the semiconductor integrated circuit comprising:

a digital sampler configured to sample the received broadcast signal to produce a serial digital bit stream at a first clock rate;

a sample reducer arranged to receive the serial digital bit stream and to combine groups of N samples to produce a reduced serial digital bit stream;

a serial to parallel converter arranged to convert the reduced serial digital bit stream to a parallel bit stream of words comprising M bits, and to output the M bit words at a second clock rate being higher than the first clock rate; and

a correlator arrangement arranged to receive the parallel bit stream of M bit words and to correlate in parallel with a locally generated version of the known digital code by correlating one of the M bit words of the parallel bit stream with an M bit word of the locally generated version of the known digital code every cycle of the second clock, wherein an increase in throughput correlation speed is achieved.

2. A semiconductor integrated circuit according to claim 1 wherein the sample reducer comprises a first shift register into which the serial digital bit stream is shifted N samples at a time at the first clock rate.

3. A semiconductor integrated circuit according to claim 2 wherein the sample reducer further comprises a bit counter arranged to count a group of bits in the first shift register and determine a number of bits having a given logic state to produce a bit count.

4. A semiconductor integrated circuit according to claim 3 wherein the sample reducer further comprises a threshold detector arranged to receive the bit count and to produce a 1-bit signal indicative of whether the bit count is greater than a given threshold, to produce the reduced serial digital bit stream.

5. A semiconductor integrated circuit according to claim 4 wherein the bit counter and threshold detector are programmable to set respectively the number of bits counted and the threshold.

6. A semiconductor integrated circuit according to claim 5 wherein the number of bits counted is selectively 7, 9, 11, 13 or 15 bits.

7. A semiconductor integrated circuit according to claim 1 wherein the serial to parallel converter comprises a memory arrangement arranged to receive the reduced serial bit stream and to output M bit words at the second clock rate.

8. A semiconductor integrated circuit according to claim 7 wherein the memory arrangement comprises a second shift register arranged to receive the reduced serial bit stream and to output M bit words.

9. A semiconductor integrated circuit according to claim 8 wherein the memory arrangement comprises first and second circulating shift registers arranged to circulate the M bit words at the second clock rate for output to the correlator arrangement.

10. A semiconductor integrated circuit according to claim 9 wherein the first and second circulating shift registers are arranged wherein one of the first and second circulating shift registers receives a stream of M bit words from the second shift register, while the other circulates at the second clock rate.

11. A semiconductor integrated circuit according to claim 9 wherein the first and second circulating shift registers each have a word depth of a plurality P words.

12. A semiconductor integrated circuit according to claim 11 wherein the first and second circulating shift registers are arranged to circulate each of the plurality P of M bit words many times at the second clock rate.

13. A semiconductor integrated circuit according to according to claim 1 wherein the correlator arrangement comprises a store which stores a local version of the known digital code.

14. A semiconductor integrated circuit according to according to claim 13 wherein the store is arranged to store the local version of the known digital code as a plurality P of M bit words.

15. A semiconductor integrated circuit according to claim 14 wherein the correlator arrangement comprises a comparison arrangement arranged to compare the M bit words of the parallel bit stream with M bit words of the local version of the known digital code.

16. A semiconductor integrated circuit according to claim 15 wherein the comparison arrangement is arranged to receive a different one of the M bit words of the parallel bit stream each clock cycle of the second clock rate and to compare one of the M bit words with a local stored version of the known code.

17. A semiconductor integrated circuit according to claim 16 wherein the local version of the known digital code is stored as a plurality P of M bit words, and every P clock cycles of the second clock rate each M bit word of the local version of the code is shifted one bit with respect to the M bit words of the parallel bit stream.

18. A semiconductor integrated circuit according to according to claim 15 wherein the comparison arrangement comprises parallel XOR gates.

19. A semiconductor integrated circuit according to claim 1 wherein the known digital signal is a repeated code signal having a code repeat period, code length and a code frequency, and wherein the sample reducer, serial to parallel converter and correlator arrangement are arranged to perform all possible correlations in the code repeat period.

20. A semiconductor integrated circuit according to claim 1 wherein the known code is a GPS code.

21. A semiconductor integrated circuit according to claim 1 wherein N = 8.

22. A semiconductor integrated circuit according to claim 1 wherein M = 66.

23. A semiconductor integrated circuit according to claim 1 wherein the first clock rate is substantially 16 MHz.

24. A semiconductor integrated circuit according to claim 1 wherein the second clock rate is substantially 64 MHz.

25. A semiconductor integrated circuit according to claim 1 wherein the increase in correlation speed is N x M x second clock rate/first clock rate.

26. A system to process a received signal of a type having a digital code, the system comprising:

a sampler unit to sample the received signal to produce a serial digital bit stream at a first clock rate;

a sample reducer unit coupled to the sampler unit to receive the serial digital bit stream and to combine groups of samples to produce a reduced serial digital bit stream;

a converter unit coupled to the sample reducer unit to convert the reduced serial digital bit stream to a parallel bit stream of words and to output the words at a second clock rate; and

a correlator unit coupled to the converter unit to receive the parallel bit stream of words and to correlate one of the words in parallel with a word of the digital code for a plurality of cycles of the second clock rate.

27. The system of claim 26, further comprising a frequency handling unit coupled to the correlator unit to correct frequency errors in a correlation throughput from the correlator unit.

28. The system of claim 27, further comprising an integration unit coupled to the frequency handling unit to sum outputs of the frequency handling unit with accumulated output values.

29. The system of claim 26 wherein the sampler reducer unit includes:

a first shift register;

a bit counter coupled to the shift register;

a threshold detector coupled to the bit counter; and

a second shift register coupled to the threshold detector.

30. The system of claim 26 wherein the converter unit comprises a serial to parallel converter having a pair of circulating shift registers.

31. A method to process a received signal of a type having a digital code, the method comprising:

sampling the received signal to produce a serial digital bit stream at a first clock rate;

combining groups of samples to produce a reduced serial digital bit stream;

converting the reduced serial digital bit stream to a parallel bit stream of words and outputting the words at a second clock rate; and

correlating one of the words in parallel with a word of the digital code for a plurality of cycles of the second clock rate to increase correlation throughput.

32. The method of claim 31, further comprising:

correcting frequency errors in the correlation throughput and producing an output; and

summing outputs with accumulated output values.

33. The method of claim 31, further comprising locally generating a version of the digital code.

34. A system for processing a received signal of a type having a digital code, the system comprising:

a means for sampling the received signal to produce a serial digital bit stream at a first clock rate;

a means for combining groups of samples to produce a reduced serial digital bit stream;

a means for converting the reduced serial digital bit stream to a parallel bit stream of words and outputting the words at a second clock rate; and

a means for correlating one of the words in parallel with a word of the digital code for a plurality of cycles of the second clock rate to increase correlation throughput.

35. The system of claim 34, further comprising:

a means for correcting frequency errors in the correlation throughput and producing an output; and

a means for summing outputs with accumulated output values.